CMOS RF Circuits for Integrated Wireless Systems

Robert H. Caverly[1], Scott Smith[2], Jiangang Hu[1], Robert Nichols[2]

[1]ECE Department
Villanova University
Villanova, PA 19085

[2]ECE Department
Univ. Massachusetts Dartmouth
N. Dartmouth, MA 02747

Abstract

There is increasing interest in the use of CMOS circuits for highly integrated high frequency wireless telecommunications systems. This paper presents the results of on-going work into the development of a cell library that includes many of the circuit elements required for the high frequency sub-system of a communications integrated circuit. The cells were fabricated using standard CMOS processes and measurement results are presented. No post processing was used with the circuits described. The full design files, testing results and circuit tutorials describing the cells are available from the author.

Introduction

The use of analog CMOS circuits at high frequencies has garnered much attention in the last several years [1-5]. At the heart of rapid prototyping of these circuits is the concept of using a versatile library of common RF function blocks. In the design of this library, the cells must be designed to be flexible in terms of drive requirements and loading. For RF applications, the most common driving requirements for off-chip loads are based on 50Ω source and load impedances. At the same time, since these cells are to be used with digital and baseband analog systems, they must be designed to be controlled by on-chip digital and analog signals. The cells described in this paper can be used separately or combined to construct more complex functions such as an RF front end. As additional assistance to the RF design community, the layout files, test data and tutorials will be available from the author.

General Fabrication Comments

All the cells being investigated were fabricated using 2.0, 1.2 and 0.8 micron (μm) silicon CMOS n-well processes using both n-channel and p-channel enhancement MOSFETs through the MOSIS fabrication service. There was no post-processing performed on any of the circuit topologies presented in this paper. Many of the designs utilized multiple gate fingers to help reduce parasitic capacitance in an effort to improve the frequency response.

The Library Elements

RF Control Element

Typical applications of the RF control element would be the sharing of a single antenna between receiver and transmitter (T/R switch), or in signal amplitude control as an attenuator. Figure 1 shows a schematic of the CMOS control element, which is similar to other FET-based elements [6]. Each gate finger of the switching element varied in width depending on the process used, from 4000 μm for the 2.0 μm process to 400 μm for the 0.8 μm process. The 0.8 micron switching element without contacts is approximately 100 by 85 microns. The larger gate length switch elements need to be physically larger since the smaller transconductance requires larger FETs to maintain low insertion loss in the switch on-state. The increased FET size negatively impacts the off-state isolation because of the increased capacitance.

RF Performance

Switch measurements were performed on a combination of unpackaged and packaged experimental SPDT chips at frequencies to 2.0 GHz. Figure 2 shows the results of isolation and insertion loss measurements on the 0.8 micron

0-7803-4471-5/98/$10.00 (c) 1998 IEEE

SPDT CMOS switching elements. All three switch technologies exhibit low frequency insertion loss values less than 0.8 dB. Isolation for all the devices is greater than 50 dB at low frequencies. Performance data for the 0.8 μm device, the best technology of the three studied, shows 3 dB insertion loss and greater than 25 dB isolation at 1.0 GHz. Measurements on the 1.2 and 0.8 micron control elements using a control voltage of 3.3 volts showed negligible differences in insertion loss and isolation over the frequency range. This lower control voltage makes these devices attractive for battery power applications.

Distortion performance was also measured for the CMOS SPDT switch element. Measurements on the 1.2 micron element yielded distortion intercept point IP2 and IP3 values of approximately +39 dBm and +27 dBm, respectively, at 110 MHz, comparable to intercept points for GaAs MESFET switches [7,8].

Series Reflective Attenuator Element

The CMOS control element was also tested in a series reflective configuration. Figure 3 shows the results of these measurements at 100 MHz on the 1.2 micron element, indicating a useful attenuation range up to 10 dB. The data are plotted with an attenuation model for comparison. Note the minimal change in element characteristics over the 3 to 5 volt range, validating the use of these devices at lower control voltages.

CMOS RF Amplifiers

Both single and differential input/output RF amplifiers (Figure 4) were designed to drive 50Ω loads. In an effort to improve the frequency response, multiple gate fingers were used which. varied in widths of 5000 μm for the 2.0 μm process, 3000 μm for the 1.2 μm and 2000 μm for the 0.8 μm process.

RF Performance

RF measurements on the packaged 2.0 and 1.2 μm single ended amplifiers were performed up 900 MHz. Measurements show RF power outputs of up to +10.5 dBm using a +5.0 volt power supply are feasible. Figure 5 shows the results of gain measurements and SPICE simulations on the 1.2 μm RF amplifiers. The current source bias (p-FET) and driver bias (n-FET) were varied to achieve the optimum gain. The 2.0 micron element showed similar low frequency insertion gain but a unity gain frequency of approximately 500 MHz.

Distortion measurements taken at 135 MHz on the 1.2 μm RF amplifier as a test of the amplifier's linearity show second, third and fourth order intermodulation intercept points (referenced to the load) of 44 dBm, 23 dBm and 19 dBm, respectively.

Measurements were also taken on a silicon CMOS SPDT switch-RF amplifier configuration feeding a 50 Ω load such as would be seen in an RF front-end application. The bias FET was adjusted for maximum output power to the load. As expected, the insertion gain of the switch-amplifier combination was reduced by the insertion loss of the switch (from approximately 14.5 dB to 13.75 dB). The second and third order intercept points of the switch-amplifier combination were reduced from the values presented above by approximately 6 and 3 dB, respectively, primarily due to the distortion properties of the SPDT switch.

CMOS RF Mixers

Two different styles of balanced mixer were designed: the single balanced (Figure 6) and the Gilbert cell (Figure 7) mixers. All the mixer circuits were designed to drive 50Ω loads. At low frequencies for the balanced mixer, both technologies provided approximately 6 dB of conversion gain. At approximately 500 MHz, the 2.0 micron mixer exhibited 0 dB conversion gain, while the 1.2 micron mixer exhibited conversion gain up to approximately 950 MHz. The best conversion gain for this mixer style occurred for peak LO voltages of 1.5 volts and higher with DC gate biases greater than 2.6 volts. The measured results showed good agreement with SPICE simulations on conversion gain.

The Gilbert cell mixer (Figure 7) exhibits a conversion gain that is a function of bias and LO drive level. Figure 8 presents the dependence of conversion gain on bias and LO drive level. The 10 MHz conversion gain results (peaking at

approximately 1.8 dB) were determined from 80 MHz and 90 MHz input signals, while the 100 MHz results were determined from 800 and 900 MHz inputs.

Conclusions

This paper presented the results of on-going work done in preparing a library of 2.0, 1.2 and 0.8 micron CMOS cells for use at frequencies above 500 MHz. The results indicate that 1.2 micron library cells have a useful range that includes the cellular telephone band at 900 MHz. Higher frequency ranges are indicated using the 0.8 micron cells, including the important commercial band pertaining to global positioning systems. Lower frequency operation at IF frequencies are possible using the 2.0 micron circuits. These cells are available from the author along with full test results.

Acknowledgment

This material is based upon work supported by the National Science Foundation under Grant No. MIP-9414308. Additional assistance in measurement goes to G. Hiller of Alpha Industries, Woburn, MA.

References

1. N. Camilleri et al., "Silicon MOSFETs, the microwave device technology for the 90s", 1993 *IEEE Intl. Microwave Symp. Digest*, p. 545, 1993.

2. R.H. Caverly and G. Hiller, "A Silicon CMOS Monolithic RF and Microwave Switching Element", *Proc. 1997 European Microwave Conference*, Sept., 1997.

3. Abidi, A. "CMOS-only RF and Baseband Circuits for a Monolithic 900 MHz Wireless Transceiver", *Proceedings of the IEEE Bipolar/BiCMOS Circuits and Technology* , p 35-42 1996.

4. J. Y-C. Chang and A. A. Abidi, A 750 MHz RF Amplifier in 2-µm CMOS, *Symposium on VLSI Circuits Digest of Technical Papers*, 1993

5. J. Y-C. Chang, A. A. Abidi, and M. Gaitan, "Large Suspended Inductors on Silicon and their use in a 2-µm CMOS RF Amplifier", *IEEE Electron Device Letters*, v. 14, 1993

6. Ayalsi, Y., "Microwave Switching with GaAs FETs", *Microwave J.*, vol. 25, pp.61-71, Nov. 1982.

7. R. H. Caverly, "Distortion in GaAs MESFET Switches", *Microwave J.*, pp. 106-114, Sept., 1994.

8. R. H. Caverly , "Distortion in Broadband Gallium Arsenide MESFET Control and Switch Circuits," *IEEE Trans. Microwave Theory and Techniques*, vol. 39(4), pp. 713-717, April, 1991.

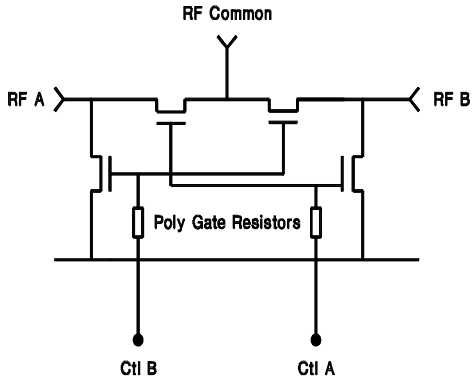

Figure 1. Schematic diagram of the CMOS microwave and RF control element.

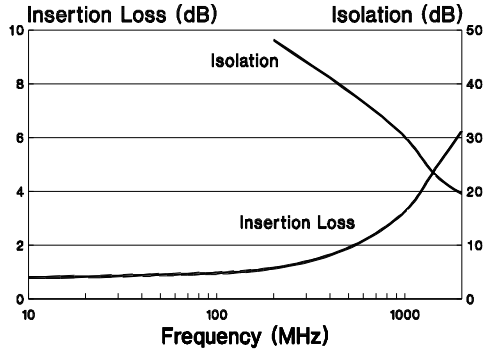

Figure 2. Insertion loss for the 0.8 micron SPDT CMOS switch. Isolation was greater than 20 dB all frequencies below 2000 MHz.

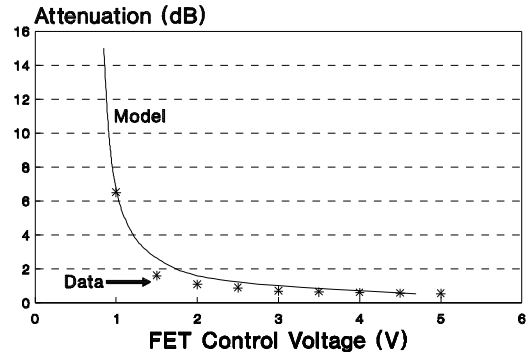

Figure 3. Attenuation characteristics of the 1.2 micron switching element in an attenuator configuration versus gate control voltage.

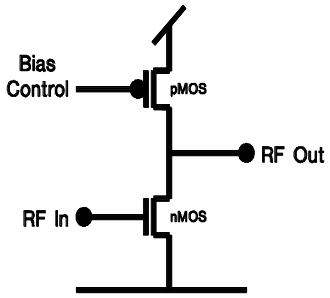

Figure 4: Single ended CMOS 50Ω RF amplifier. The differential input/output amplifier contains two identical cells.

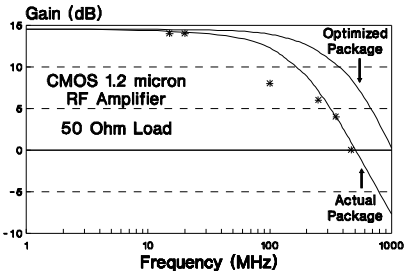

Figure 5. Frequency Response of the 1.2 μm integrated CMOS RF amplifier.

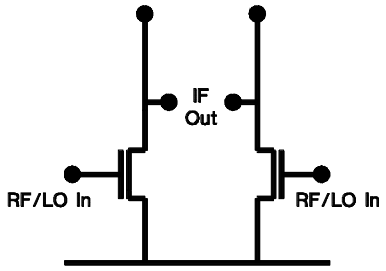

Figure 6. Schematic diagram of a general single balanced CMOS mixer.

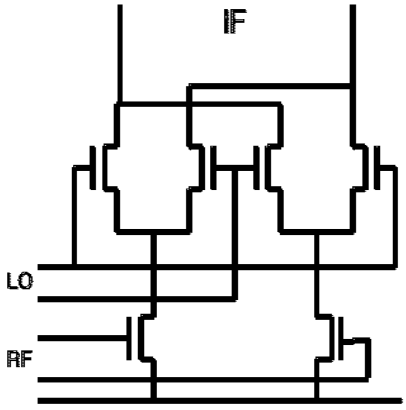

Figure 7. Schematic diagram of CMOS Gilbert cell mixer.

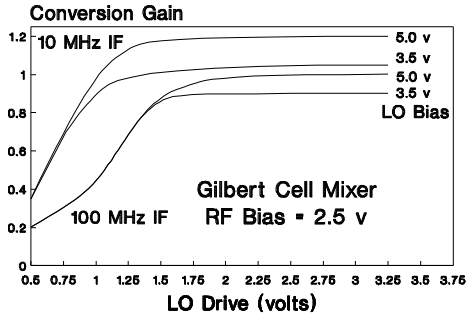

Figure 8. Conversion gain versus LO bias, IF frequency and LO drive level for the CMOS Gilbert cell mixer.